Proceedings of the 3rd International Conference on Computing Innovation and Applied Physics
DOI: 10.54254/2753-8818/14/20240913

Research on particle noise based on second-order effect

Gehui Mao

International engineering collage, Xi'an University of Technology, Xi'an, Shaanxi, 710000, China

3212231039@xaut.edu.cn

Abstract. The development of integrated circuits has gone through several stages, from the invention of transistors to the emergence of very large scale integrated circuits and system level integrated circuits. Now, the size of integrated circuits enters the nanometer level, and short-channel shot noise becomes an important issue. Short-channel shot noise increases due to factors such as device size reduction and scattering during channel formation. It has a serious impact on the performance, power consumption and reliability of integrated circuits. The formation mechanism of short channel shot noise can be explained from two aspects: one is due to the existence of thermal noise inside the channel, and the other is due to the noise caused by the shot. As the device size decreases, the channel thermal noise gradually changes into shot noise and becomes one of the main noise sources. Aiming at the noise generation mechanism, this paper proposes several methods to solve the short-channel shot noise. Through the research of short-channel shot noise and the exploration of solutions, the impact of shot noise on IC performance can be better understood and dealt with, and the development and innovation of IC technology can be promoted.

Keywords: Second Order Effect, Short Channel, Shot Noise, Field Effect Transistor.

1. Introduction

The development of integrated circuits is the basis for driving the development of modern information technology, and its development process can be divided into several stages: First stages is the invention of the transistor in the 1950s. William Shockley, John Bardeen, Walter Brattain successfully made the first transistor at Bell Labs, which replaced the early vacuum tube technology and made electronic devices smaller and more reliable. Small-scale integrated circuits (SSI) in the 1960s, in which several (usually ten to hundreds) transistors were integrated onto a chip, forming small-scale integrated circuits. The circuits were primarily employed in digital logic systems, such as calculators and early computers. During the 1960s-1970s, medium-scale integrated circuits (MSI) emerged, incorporating hundreds to thousands of transistors onto a single chip to create medium-scale integrated circuits. Subsequently, in the 1970s, large-scale integrated circuits (LSI) were developed with the integration of thousands to hundreds of thousands of transistors onto a chip, resulting in the formation of large-scale integrated circuits. Very large-scale integrated circuits (VLSI) in the 1980s, in which hundreds of thousands to millions of transistors were integrated onto a chip, forming very large-scale integrated circuits. Ultra-large-scale integrated circuits (ULSI) and system-on-chip (SoC) from the 1990s to the present. Abstract: With the development of integrated circuits and transistors to

© 2023 The Authors. This is an open access article distributed under the terms of the Creative Commons Attribution License 4.0 (https://creativecommons.org/licenses/by/4.0/).

DOI: 10.54254/2753-8818/14/20240913

the current nano level, more problems have emerged, such as the noise interference in MOSFET devices. The reduction in dimensions of metal-oxide semiconductor field effect transistor (MOSFET) devices has led to an excessive presence of noise observed in short channel MOSFET devices. Short channel scattering noise is an important challenge and research field in the design and manufacture of integrated circuits. With the continuous reduction of the scale of integrated circuits, the rapid reduction of device size, and the continuous increase of operating frequency, the problem of short channel scattering noise has become particularly prominent. Short channel scattering noise is mainly caused by the thermal movement, current disturbance and energy scattering of electrons in semiconductor materials, which has a serious impact on the performance, power consumption and reliability of integrated circuits. There are two primary perspectives regarding the factors contributing to excessive noise: one suggests that the device's short channel effect leads to an increase in channel thermal noise, resulting in excessive noise; while the other proposes that scattering noise is responsible for its occurrence. In long channel MOSFET devices, carriers enter the channel from the source terminal and undergo multiple scattering under the influence of electric fields before reaching the drain terminal. The formation of a channel resistance due to this scattering process gives rise to thermal noise within the device's channel. Thermal noise predominantly accounts for long-channel devices' channel noise. However, as MOSFET devices shrink below 40nm, carrier transport mechanisms gradually shift from drift-diffusion transport to quasi-ballistic or even ballistic transport [1]. Consequently, carriers entering the device's source face energy barriers at the interface of its channels, leading to potential barrier-related scattering noises within them [2, 3]. For long channel MOSFET devices, there is almost no existence of potential barrier when the carriers enter the channel from the source, so there is basically no scattering noise [4]. With the size of MOSFET devices entering dozens of nanometers and continuously decreasing, the mechanism of channel noise of devices begins to change gradually from thermal noise to scattering noise, and the proportion of scattering noise in channel noise gradually increases, becoming one of the main reasons for excessive noise in the channel [4]. Through the research and exploration of short channel scattering noise and solutions, we can better understand and deal with the impact of scattering noise on the performance of integrated circuits, and promote the development and innovation of integrated circuit technology. At the same time, it also provides a direction for the study of materials science to solve the impact of noise.

This document is structured into three sections: commencing with an introduction that primarily discusses the evolution of integrated circuits and transistors, it subsequently highlights the research problem at hand. The second part is the analysis of the problem, analyzes the causes of noise in MOSFET devices short channel, and introduces the corresponding second-order effect. The third part is to put forward theoretical solutions, according to the analysis of the problem in the second part, puts forward the corresponding solutions. The fourth part is the summary, describes the results of the study and the prospect of the future study.

2. Second order effect

When the size of the MOSFET device is reduced to 90nm, there is a more pronounced impact on the device due to second-order effects. This results in an increased level of noise for short channel devices compared to long channel devices. Second-order effects refer to various circuit operation phenomena that occur in integrated circuits using MOSFETs, including channel length modulation, short channel effect, body effect, and subthreshold conductivity effect. The focus of this paper is primarily on studying the influence of short channel effect and channel length modulation effect on the device as well as their contribution to scattered noise.

2.1. Channel length modulation effect and short channel effect

The MOSFET transistors demonstrate the phenomenon of channel length modulation, where the position of the channel beneath the gate slightly shifts towards the source terminal as Vds continues to increase. As a result, there is a marginal decrease in the effective resistance of the channel, facilitating an enhanced drift of electrons from the source terminal to the channel region. This leads to an

DOI: 10.54254/2753-8818/14/20240913

increased accumulation of drift electrons within the depletion region and subsequently amplifies Id [5]. The application of this effect can be seen in modems used for wireless communication systems like FM modem and AM modem. These modems utilize MOSFET's channel length modulation effect to achieve high-quality signal transmission and reception with low power consumption and high sensitivity. However, it should be noted that this effect may introduce nonlinear distortion and can be sensitive to noise and interference induction, potentially affecting signal quality. Additionally, shortening the channel length has become a common practice in chip design for improved process technology and performance. Nevertheless, this also introduces changes such as sub-threshold swing alteration, threshold voltage adjustment, increased quasi-static power consumption, and modified transmission characteristics [6]. It is important to consider that shorter channels generate different types of noise compared to longer channels; specifically transitioning from thermal noise to particle noise [7], which significantly impacts circuit performance [8].

2.2. *Principle derivation*

Figure 1 is a schematic diagram of the structure of NMOSFET devices. The overall coordinates are drawn with the junction of the source pole and the device channel as the origin. The X axis direction is the direction perpendicular to the channel along the source pole pointing to the substrate. The Y axis direction is set perpendicular to the X axis and extends along the channel, pointing from the source pole to the drain pole. The value of Y represents the coordinates of the electron in the channel. In Figure 1, L1 represents the electrical channel length, L2 represents the effective channel length, and ΔL represents the change in channel length caused by the channel length modulation effect. In NMOSFET devices, due to the influence of channel length modulation effect, the channel of NMOSFET devices is usually divided into two zones:

(1) the area of 0≤Y≤L1 is called the linear channel area, which is the area where the electron channel is located [6];

(2) the area of L1≤Y≤L2 is called the velocity saturation area [9], Y=L1 is the clip point, also called the saturation voltage point, and the voltage VDS(Y=L1)= VDSAT is the saturation voltage [6] In Fig. 1, when VDS≥VDSAT, the excess drain-source voltage (VDS-VDSAT) is applied to the velocity saturation region on the right side of the channel. Due to the influence of drain-source voltage VDS on electrical channel length L1, it can be considered that the length of the electrical channel is "modulated" by this voltage. As shown in Fig. 1, within the inversion layer of the device, a transverse electric field EY is induced by drain-source voltage in the transistor's channel with its direction pointing from drain to source; meanwhile, a longitudinal electric field EX perpendicular to EY is generated by grid voltage and its direction points from SiO2-substrate interface towards substrate [6]. The transverse electric field EY in turn leads to depletion region formation around device's drain pole which serves as root cause for MOSFET devices' channel length modulation effect. Although such effect also exists in long-channel devices, their drain depletion region width is much shorter compared to short-channel devices (as depicted in Fig. 1 where ΔL is negligible compared with effective channel length L2). However, for short-channel MOSFET devices due to reduced size, transverse electric field within their channels becomes stronger resulting in increased width of drain depletion region and significant difference between ΔL and L2 lengths leading to substantial reduction in electrical channel length L1. In comparison with long-channel devices, this modulation effect has notable impact on current-voltage characteristic curve regardless whether it operates within linear or saturated regions.

DOI: 10.54254/2753-8818/14/20240913

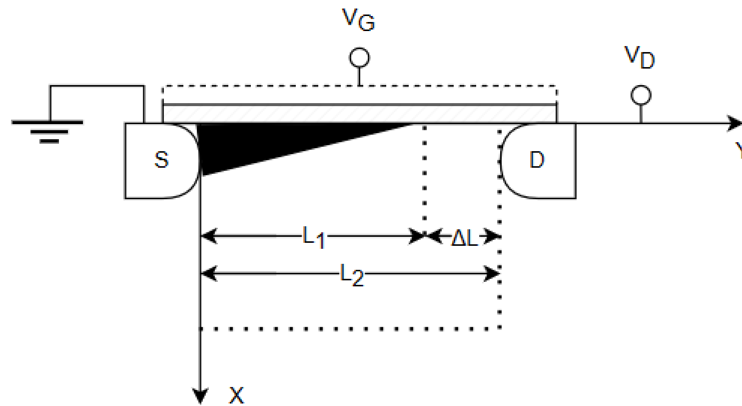

Figure 1. Schematic diagram of the NMOSFET device.

3. Particle noise

1. The generation of noise in FETs is primarily attributed to carrier dispersion, which predominantly occurs in junction devices such as diodes and electron tubes. This is due to the presence of potential barriers within these devices, causing carriers to pass through them independently and randomly. Such noise resulting from independent and random carrier passage across potential barriers is referred to as "noise" [10]. In FETs, both the Fermi effect and Coulomb effect exist, effectively suppressing this noise. Consequently, the noise can be categorized into two types: full noise and suppressed noise. The following formula represents the expression for calculating the noise [8], where IDS denotes source leakage current, q represents electron charge, and F signifies the inhibitory factor of noise. When F equals 1, it indicates full noise; when F is less than 1, it implies suppressed noise [8, 11]. The inhibitory factor of noise reflects the extent of suppression against unwanted disturbances [12].

$$S = F \cdot 2qIDS$$

When MOSFET devices are in operation within the strong inversion region, they effectively mitigate speckle noise. However, when operating in the weak inversion region, speckle noise is converted into complete scattering noise, emerging as the primary source of interference for these devices [13, 14].

4. Low noise thinking

Given the impact of particle noise on devices with shorter channels, it becomes crucial to effectively mitigate this type of interference. The occurrence of particulate noise is attributed to carriers near the source area being constrained by the channel barrier during injection. Therefore, enhancing the emissivity and carrier correlation in the source area can effectively suppress particulate noise. This can be achieved by increasing the cross-sectional area of the source region, elevating the concentration of source-leakage doping, and improving carrier injection speed. Additionally, both Fermi effect and Coulomb effect contribute to suppressing particulate noise; thus, these two effects should be strengthened accordingly. The strength of Fermi effect is directly proportional to carrier degeneracy which can be enhanced through heavy doping in the source-leakage region. In contrast, interaction among carriers in the channel region can be improved by increasing gate voltage to enhance suppression effect. Moreover, doping and gate voltage in the source-leakage region also promote Coulomb effect for further reduction of particulate noise. Furthermore, considering scattering noise from its essence perspective, reducing height of channel barrier helps minimize random scattering of carriers and consequently mitigates particulate noise impact as demonstrated in literature [15]. Henceforth, increasing leakage bias could be employed to inhibit particulate noise.

DOI: 10.54254/2753-8818/14/20240913

5. Conclusion

This paper aims to investigate the particle noise in nano-MOSFET devices by utilizing the theory of particle noise suppression. The dominant noise in MOSFET devices undergoes a transition from thermal noise to particle noise, while the carrier transport mode shifts from diffusion-drift transport to quasi-ballistic transport due to the reduction of channel length from long channel to short channel. Therefore, this paper examines the effects of channel length modulation and short channel on second-order effects based on short-channel MOSFET devices, briefly discusses their applications in devices, and deduces the reasons behind their emergence. Furthermore, this paper explores the generation mechanism of particle noise in nano-MOSFET devices and establishes an internal relationship between changes in main noise and alterations in transport mechanisms within MOSFETs, thereby deriving both main noise generation mechanism and transport mechanism. Based on these findings, strategies for reducing noise in short channels are proposed: increasing source area injection cross-section area, employing high doping source leakage, using low doping channels, and raising gate voltage can effectively achieve low-noise operation of nano-MOSFET devices.

References

[1] Jia X F, Du L, Tang D H, Wang T L, Chen W H, 2012, Acta Phys. Sin. 61 127202
[2] Do V A, Dollfus P, Nguyen V L 2007 J. Comput. Electron. 6 125
[3] Navid R 2007 J. Appl. Phys. 101 124501
[4] Jia X F, He L 2017 AIP Adv. 7 055202.
[5] Liu N Z, Zhang X B, Yao R H. AlGaN/GaNA physical model of the capacitance at the outer edge of a device with high electron mobility[J].Chinese Journal of Physics, 2020, 69(07):262-270.
[6] Zhang M. Thermal Noise Modeling for Short Channel Field Effect transistors[D].South China University of Technology,2021.DOI:10.27151/d.cnki.ghnlu.2020.000251.
[7] Xiaofei Jia, Liang He; Research of shot noise based on realistic nano-MOSFETs. AIP Advances 1 May 2017; 7 (5): 055202.
[8] Zhang M,Yao R H,Liu Y R , Geng K W. Shot noise model of the short channel metal-oxidesemiconductor field-effect transistor[J]. Chinese Journal of Physics,2020,69(17): 351-359.
[9] Asgaran S, Deen M J, Chen C H. Analytical Modeling of MOSFETs Channel Noise and Noise Parameters[J]. 2004,51(12): 2109-2114.
[10] Wang T L. Study on shot noise and transport mechanism of nanometer MOSFETs[D].University of Electronic Science and Technology of China, 2012.
[11] Do, V.N., Dollfus, P. & Nguyen, V.L. Shot noise in resonant tunneling diodes using the non-equilibrium Green's functions calculation. *J Comput Electron* 6, 125–128 (2007).
[12] X. Chen, C. -H. Chen and R. Lee, "Fast Evaluation of the High-Frequency Channel Noise in Nanoscale MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1502-1509, April 2018, doi: 10.1109/TED.2018.2808184.
[13] L. H. K. Chan *et al.*, "MOSFET Drain Current Noise Modeling With Effective Gate Overdrive and Junction Noise," in *IEEE Electron Device Letters*, vol. 33, no. 8, pp. 1117-1119, Aug. 2012, doi: 10.1109/LED.2012.2203781.
[14] Heng-Fa Teng, Sheng-Lyang Jang, M.H. Juang,A unified model for high-frequency current noise of MOSFETs,Solid-State Electronics,Volume 47, Issue 11,2003,Pages 2043-2048,ISSN 0038-1101.
[15] Xiao T,Qiao J L,Chen J,Yang J H.Analytical model of barrier height for P-N junction type depletion channels[J].Chinese Science Bulletin,2017,62(Z2):3392-3399.