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Source of IC power consumption and low power design

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Abstract. In these years, with the continuous development of 14nm and 7nm chip processes and the increasing popularity of computers, cell phones, and smart homes, the growing market of electronic products and ultra-fine research for the reliability of the chip requirements gradually increased. The method of reducing power consumption in the new context of new technology is called the chip field die-cut concern. This paper mainly summarizes two aspects of power consumption sources and methods to reduce power consumption, to provide a reference basis for future research directions: First, the major sources of power consumption are static power consumption and dynamic power consumption. The primary sources of static power consumption are sub-threshold leakage and gate leakage current. This paper also mentions some other leakage currents, such as reverse bias PN junction current and induced leakage current, which can be more carefully considered when exploring methods to reduce power consumption. A more comprehensive consideration when exploring ways to reduce power consumption. Dynamic power consumption is mainly divided into Switching power and Internal power and short-circuit power. Then we summarize the existing methods which can reduce power consumption: Clock gating (including Clock gating without a latch and Clock gating with a latch), Dynamic voltage and frequency scaling, multi-supply and multi-voltage technology, Power gating and multi-threshold voltage. These methods are from a proprietary perspective to reduce power consumption.

Keywords: Static and Dynamic Power Consumption, Clocking Gating, Power Gating.

1. Introduction

1.1. Background

The advent of the electron tube marked the world's development towards integration and globalization. In 1946 the first electronic computer ENIAC was designed. The internal circuit of that has 500,000 welding points, power consumption of more than 174 kilowatt hours. Worth concern is that the electronic tubes burn out every 15 minutes on average. Therefore, based on such a large power

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consumption and volume, transistors gradually replaced electron tubes using the advantages of their low power consumption and small size. The first known transistorized computer, TRADIC, carry out 1 million logic operations per-second with merely one hundred watt-hours of power, greatly increasing efficiency and reducing power consumption.

It can be seen that the problem of power consumption is actually a very important issue to be solved in the modern electronics industry.

Currently, more and more components are integrated into a semiconductor chip, and the size of the chip becomes smaller at the same time, gradually powerful. In this process, reducing power consumption while maintaining the performance of high-performance, high-speed chips is becoming a primary issue.

1.2. Problems and Benefits

High power consumption of integrated circuits mainly brings two problems, one is the heat problem, and the other is the problem of heat dissipation. High power consumption of the chip in the work of the chip will quickly heat up. Working for a long time at high temperatures will also reduce its service life and performance [1]. At the same time, thermal problems can also affect the reliability of integrated circuits by stimulating a variety of minor physical defects and time delay failures; It will also increase the manufacturing difficulty of the chip. This is because the thermal conductivity of ceramics is better than plastic, and the coefficient of thermal expansion of ceramics is low, so the reliability of chips using ceramic packages is relatively high. So, we need to change the materials from low-cost plastic packages to expensive ceramic packages.

Research on how to reduce power consumption has many benefits. Firstly, solving the above heat generation problem and heat dissipation problem can improve the reliability of the chip. Secondly, existing research and solutions to high power consumption problems can provide directions and methods for further integrated circuits.

2. Static Power Consumption

Generally speaking, in an ideal CMOS, there is no leakage current at a static state, i.e., no static power consumption. However, in practice, multiple leakage currents are present, which introduce excess static power consumption. This is why the static power consumption also becomes the leakage current power consumption.

In the IC static power consumption, there are four main types of leakage current: subthreshold leakage, reverse bias PN junction current, gate leakage current, and induced leakage current.

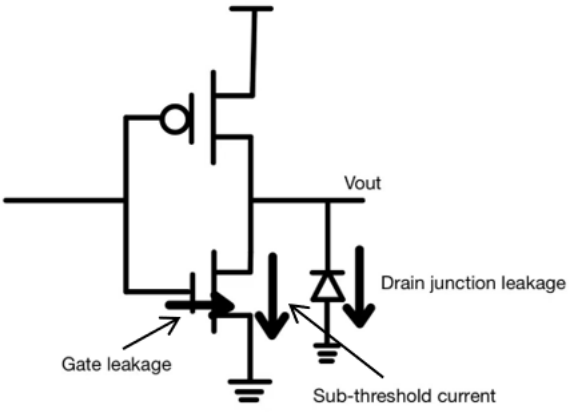

Figure 1. Source of static power consumption.

Figure 1 shows three of the four main sources of static power consumption.

The first is the largest proportion of the total static power consumption: subthreshold leakage current, the reason is that the CMOS is not completely off, and the leakage current from the source to the drain.

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It is worth noting that there is a relationship between the sub-threshold current and the threshold voltage is exponential, which means the sub-threshold current will vary significantly with the threshold voltage, while the sub-threshold current will also exceed the target value under some extreme physical conditions in the outside world.

The second is the reverse bias PN junction current, which is the current form due to the lesser drift and electron-hole pairs in the reverse bias PN junction formed by the source-drain region and the substrate.

The third is gate leakage current, which is the leakage current from the gate via the oxide layer to the substrate due to the tunneling phenomenon and hot carrier effects. In 90 nm processes, the gate leakage current has reached one-third of the subthreshold current, and in some cases, the gate leakage current can even reach the same level as the subthreshold current.

The fourth is the induced leakage current between the gate and the drain. The leakage current from the drain to the substrate region when high voltage is added to IC.

In some cases, there are other secondary effects induced leakage currents, such as DIBL effect-induced sources and drain, Thermionic effect induced by the thin gate oxide layer, and Thermionic effect-induced substrate current [2].

3. Dynamic Power Consumption

CMOS circuits usually dissipate dynamic power in the following two cases:

1. When NMOS and PMOS carry on current during signal conversion, PMOS and NMOS transistors will conduct simultaneously for a short period if the logic changes its states [3]. The circuit is temporarily shorted at this point, resulting in power loss.
2. With the switching movements at the nodes, the switching movement is the alteration in the logic state of a circuit node and the probability of switching from logic 0 to logic 1 or logic 1 to 0, considered as the activity factor.

Generally, the dynamic power consumption caused by high switching activity circuits is higher than that caused by transient short-circuit current paths [4]. Therefore, the focus should be on finding ways to reduce the switching power.

3.1. Switching Power

Switching power consumption is related to voltage, flip rate, and load capacitance.

Switching power is independent of the data. That is, the transferred data will not affect the flip power consumption, but the flip rate of the data will affect the flip power consumption. The switching power is shown in Figure 2.

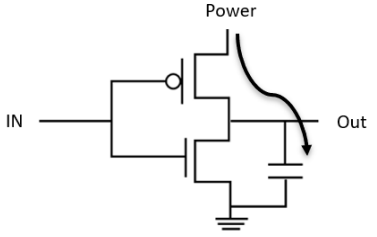

Figure 2. Switching power.

3.2. Short-circuit Power

Short-circuit power can also be called internal power consumption, which is predominantly created by short circuits. Typically, there is a time when PMOS and NMOS are turned on simultaneously, during which DC equal to VDD is applied to the ground, resulting in short-circuit power dissipation.

Switching power consumption plus short-circuit power consumption forms the total power consumption:

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$$P_{dyn} = \left(C_{eff} \cdot V_{dd}^2 \cdot f_{clock}\right) + \left(t_{sc} \cdot V_{dd} \cdot I_{peak} \cdot f_{clock}\right) \quad (1)$$

In equation (1), t_{sc} is the mount or decreased time of the input signal and I_{peak} is the crest current. The latter part of this equation is the short-circuit power consumption.

For the reason that the time of duration of the short circuit in the transmission is short and the short-circuit power consumption is much lower than switching power consumption. Therefore, the short-circuit power consumption will be ignored in general, and the switching power consumption will be regarded as the dynamic power consumption [5]. Then the simplified formula of the dynamic power consumption is as the equation (2):

$$P_{dyn} = C_{eff} \cdot V_{dd}^2 \cdot f_{clock} \quad (2)$$

In some cases, however, short-circuit power consumption should still be considered, such as how to deal with the dangling output of the gating module.

4. Methods of Reducing Power Consumption

4.1. Clock Gating

The clock tree consumes almost half or more of the entire chip power consumption [6], so it is crucial to control the power consumption of the clock tree. Clock gating is a technology that closes the register when the signal input is invalid, which can significantly reduce the flip power consumption [7].

4.1.1. Clock Gating without Latch. As Figure 3 shown, a gated clock circuit without latches is the simplest gated clock that can be fully implemented by a simple and/or gate [8].

Although clock gating without a latch is simple, we cannot ensure the EN duration. If the EN duration is less than T/2 (the period of the T-bit CLK), then the gating is invalid. To avoid prematurely truncating the clock pulse or mistakenly creating multiple clock pulses or burrs on the clock, proper operation forces the enable signal (EN) to be a constant from the active edge of the clock to the inactive edge of the clock.

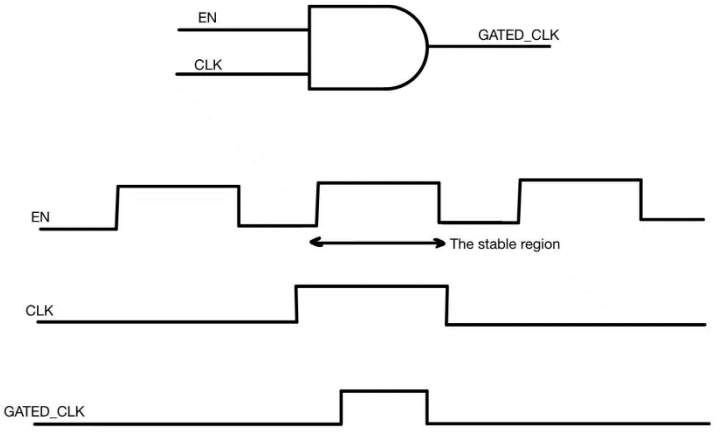

Figure 3. Clock Gating without latch.

4.1.2. Clock Gating with Latch. The latch is a logic element with a memory function in a digital circuit, which can store the signal temporarily to maintain a particular level state. The latch-based gated clock is designed to incorporate a level-sensitive latch to keep the enable signal unchanged between the active and inactive edges of the clock so it is unnecessary to rely on the gating circuit itself to meet this requirement [9]. Since the latch can seize the enable signal and hold it until a full clock pulse is generated,

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the enable signal only needs to remain stable near the active edge of the clock. However, there is no need to consider whether the setup time and hold time are violated.

When using this design approach, attention must be paid to the duty cycle of the clock as well as the delay of the enable signal logic, since the enable signal must be generated at half a clock cycle (that is, longer than half a clock cycle). Problems can occur when the logic for generating the enable signal is complex or when the clock duty cycle is out of balance (similar problems can occur when the clock duty cycle is less than 50%).

4.2. Dynamic Voltage and Frequency Scaling

Dynamic voltage and frequency scaling is a kind of dynamic technique, which means adjusting the operating frequency and voltage according to the computing power required by programs in time [10]. This technique is applied according to the following formulas (3&4):

$$P = aCV^2F \tag{3}$$

$$E = P \times t = aCV^2F \times t \tag{4}$$

It is not hard to find that lower the operating frequency can lower the power consumption. However, energy cannot be saved if we just lower the operating frequency, because, for a given task, F * t is a constant value. The energy can be saved if we lower the operating frequency and lower the voltage meanwhile. Besides the support of the chips, optimizing the software is also important. There is a typical procedure for DVFS [10]:

(1) Signals that correspond to the system performance in time, are collected in order to compute the load.

(2) Foresee the next performance, which can be decided by the current system load.

(3) Change the settings of the clock according to the prediction that is converted into the wanted frequency.

(4) Desired voltage can be known by predicted frequency, then notify the power management module to adjust the voltage to the CPU.

Pay attention to the order of adjustment when frequency and voltage are changing. If the frequency decreases, the frequency should decrease before the voltage. Nevertheless, as the frequency increases, the voltage increases before the frequency.

4.3. Multi-supply and Muti-voltage Technology

Multi-supply and Multi-voltage technology can significantly lower dynamic power consumption [11]. Multi-supply means different logic modules located in different domains powered by different sources. The use of multi-voltage technology makes some modules in the circuit work at lower voltages, and they are more susceptible to voltage drop, resulting in timing violations. The solution to the static voltage drop effect is to improve and optimize the power network. The solution to the dynamic voltage drop effect is to insert a decoupling capacitor between the power supply and the ground wire. When a large number of units in a local area of a transient circuit simultaneously turn over their signals, causing the increase of charge-discharge current in a very short time and resulting in the drop of the power track voltage, the decoupling capacitor will provide additional current to nearby units to reduce the voltage drop on the power track, thus reducing the influence of the dynamic voltage drop effect on the time sequence.

4.4. Power Gating

4.4.1. Switch Cell. In a basic CMOS circuit, leakage currents flow from VDD to the ground. A power gating circuit called switch cells could be applied to a CMOS that cuts the route from VDD toward GND, hence reducing leakage power.

A switch cell is connected to a global power supply, creating a virtual power network for the CMOS logic circuit to connect. The virtual power network is controlled by a SLEEP signal.

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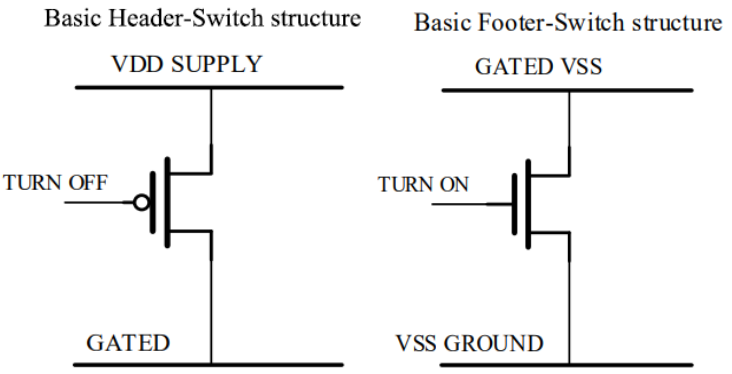

Figure 4. Header and footer switch structure.

There are two categories of switch cells, header switch cell and footer switch cell (see Figure 4). The header switch cell gates VDD rails by PMOS transistors, the footer switch cell gates VSS rails by NMOS transistors.

4.4.2. Methods. There are two power gating methods, fine-grain power gating and coarse-grain power gating.

Fine-grain power gating includes a switch cell in every single cell. It is very suitable for managing the supply. Each block could be controlled separately.

Coarse-grain power gating is more coarse. It manages several blocks by sharing a virtual supply controlled by a switch.

There are two structures of coarse-grain power gating. Ring-based and column based coarse-grain power gating. Ring-based structures put switch cells around the blocks, and column-based structures put switch cells in columns.

4.5. Multi-threshold Voltage

4.5.1. . Main Concept. According to the formula of dynamic power dissipation (equation 5):
Dynamic power dissipation is directly proportional to V_{DD}. If we managed to control V_{DD}, we could lower the power dissipation.

$$P_{dynamic} = \alpha C V_{DD^2} f \tag{5}$$

Since not all components require full voltage supply to give the best performance, we could vary the voltage supplied to each component. Components with similar voltage requirements could be grouped together as voltage islands to lower the complexity of routing.

The varying voltage between voltage islands slows the speed of the circuit, and the sampling of signal might be wrong between islands, which causes problems.

4.5.2. Level Shifters. There are either three statuses between domains: ‘always higher’, ‘always lower’ or ‘always the same’. To solve the problems, High-to-Low level shifters are used for ‘always higher’ and Low-to-High level shifters for ‘always lower’. High to low-level shifters consists of two inverters in a series.

Due to problems such as increased switching currents, slow transmission time, and crossbar current, it is more difficult to construct a Low to High-level shifter. It requires two supply rails, and shares a common ground.

5. Conclusion

This paper describes the power consumption of CMOS circuits. And the factors that affect dynamic power consumption include load capacitance, source voltage, clock frequency, and switching activity.

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And the factors that affect the static power consumption are the threshold voltage of the transistor, the width to length ratio, the oxide thickness and other process parameters and temperature. Then, based on these influence factors, we analysis and study the basic ways to reduce static power consumption and the other one (dynamic power consumption), and then raise the low-power design method, including multi-power voltage technology, multi-threshold voltage technology, clock gating technology, gated power source technology, etc. At present, driven by Moore's Law, the IC industry is becoming increasingly integrated, the tube size is becoming increasingly smaller, and the power consumption generated by the leakage current has gradually become as large as the dynamic power consumption. In the design, how to balance the dynamic power consumption and static work consumption and keeps them within a reasonable range, is an important problem facing IC design nowadays and the direction of our efforts and improvement in the future.

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Jiaqi Zhang, Lingxuan Dong, Shuo Yuan, and Junhao Gu contributed equally to this work and should be considered co-first authors.

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